A 32–bit Pipeline RISC CPU

from Verilog Code to Gata–Level Synthesis

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DISP

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Outline

Outline

Roughly Speaking...

A CPU needs:

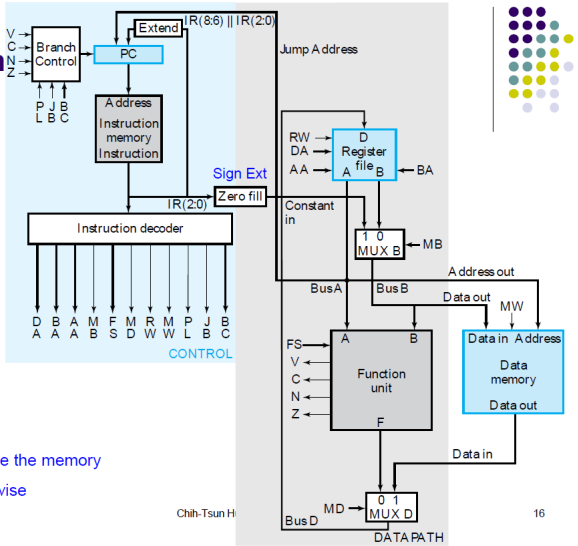
Registers: Memory Hierachy 的最上層 Storage Unit。CPU 可以直接讀取、寫入。

Instruction: CPU 聽得懂的話。以 $A + B = C$ 爲例，必須告訴 CPUA, B, C 的位置和它必須執行的運算 $'+'$。

ALU: Function Unit，執行各種運算的地方。

Cache: 比 Registers 慢一點，但容量較大的 Memory(SRAM)。現在的做法會將存 innstruction 和 data 的 cache 分開。

Block Diagram

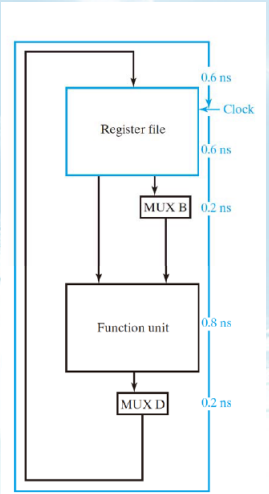


MW = 1: to write the memory

MW = 0: otherwise

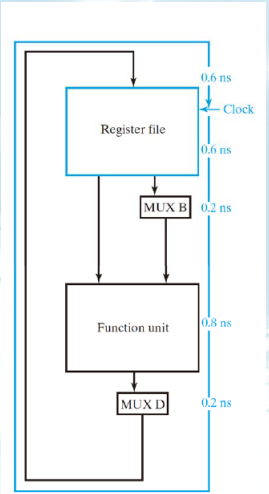
Clocks...

- 每個 Instruction 都需要數個 Clocks 來完成，包括從 Cache 讀入 Data、Instruction 到 Registers。



Clocks...

- 每個 Instruction 都需要數個 Clocks 來完成，包括從 Cache 讀入 Data、Instruction 到 Registers。
- How to increase efficiency ?



Outline – CPU Structure

閒置村民...

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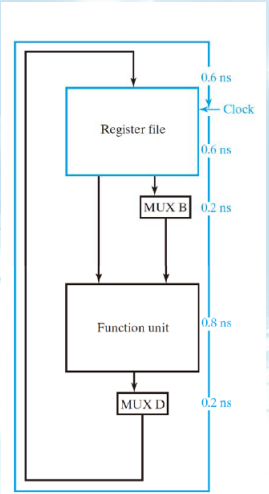

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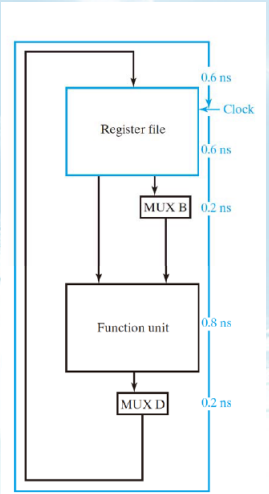

閒置村民...

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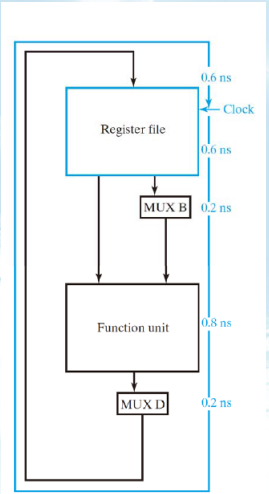
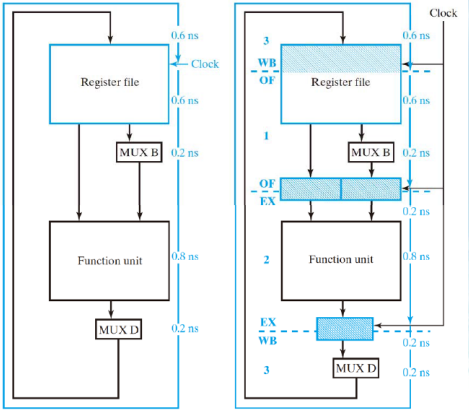
- 一起工作，不要偷懶。

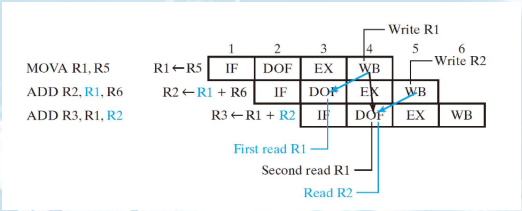


閒置村民...

- Single cycle:
  - Latency: 2.4ns
  - Max frequency:
    - 416.7MHz
- Pipeline:
  - Latency of a single operations: 2.8ns
  - Max delay between *pipeline platforms:* 1.0ns
  - Max frequency:
    - 1GHz



Hazards



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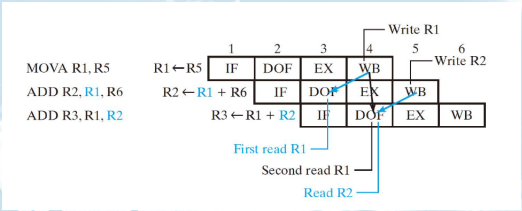
Hazards



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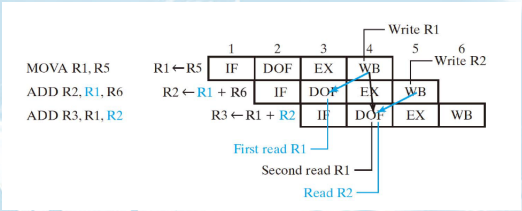

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Data Stall

Add 'bubble' to certain cycle.

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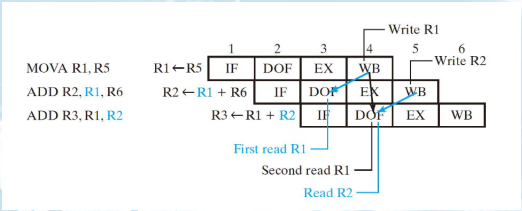

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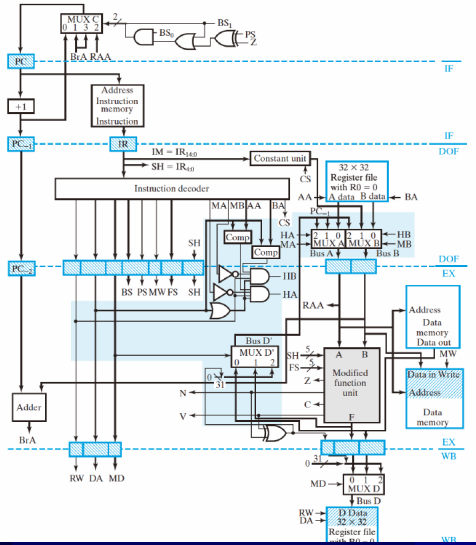
Data Forwarding

Don't wait for WB stage, just throw the computed–output to following instructions.

Pipeline CPU Structure

Pipeline RISC with Data Forwarding

- An additional MUX D' for forwarding



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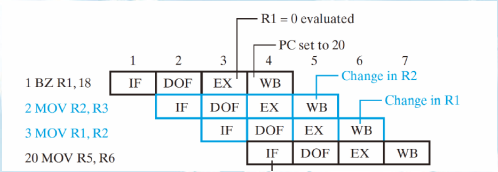
Branch–Hazard, or called Control Hazard

- After pipelined, the branch instruction has something wrong.



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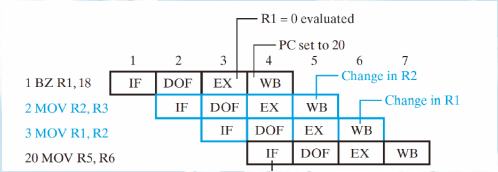
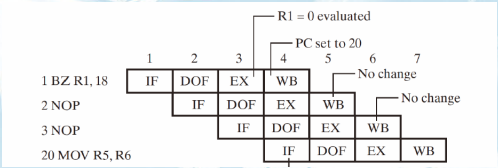


- The same strategy as Data Hazard can be taken.

Adding NOPs

- just like Data Stall.



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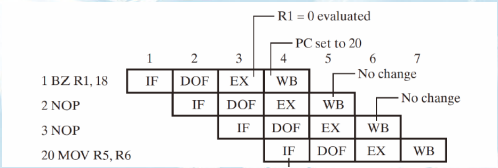
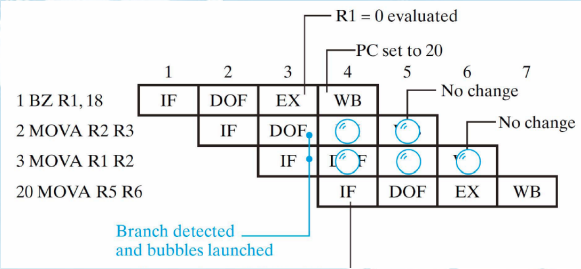


- Don't do anything before confirming branch targets.

Branch Prediction

- However, We can guess what will happen.



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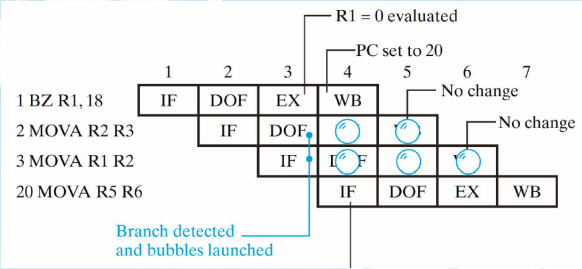
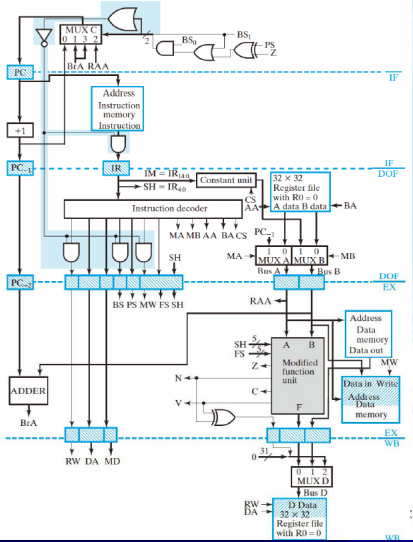


- And undo instructions if our guess is wrong.

Now the CPU looks like...

Pipeline RISC with Branch Prediction

- Branch/Jump is controlled by MUX C
  - When the selection is not zero, branch or jump occurs
- A big OR is used to clear
  - RW and MW from writing data
  - BS to stop next branch
  - IR to replace the next instruction with a NOP



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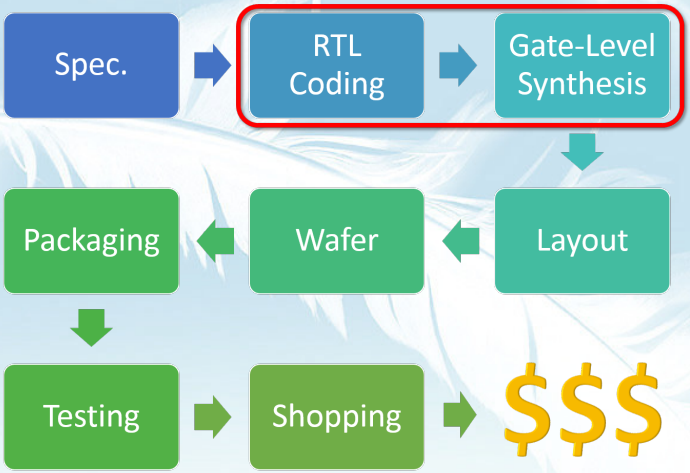
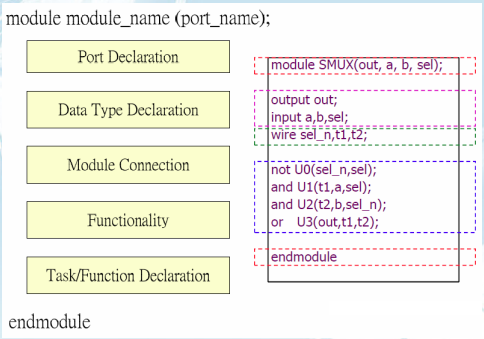
Outline

Digital IC Design Flow



RTL Coding – Verilog

- A kind of hardware description language(HDL).
- Module–Base



- alu.v
- register_file.v
- instruction_decorder.v
- risc.v

Outline – Implementation

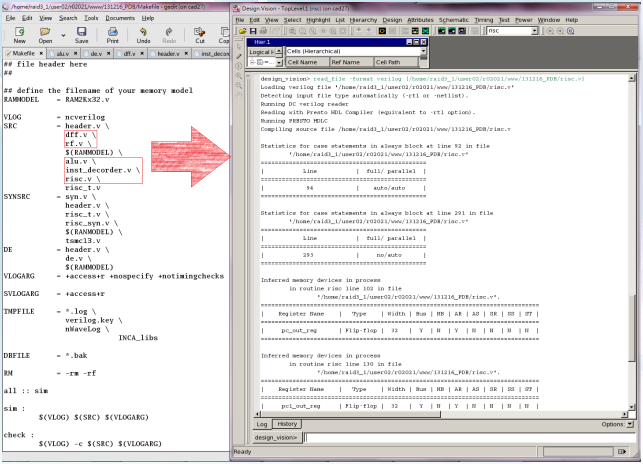
2. Implementation
   - IC Design Flow
   - RTL Coding
   - Gate–Level Synthesis

Tool Chain(EDA)

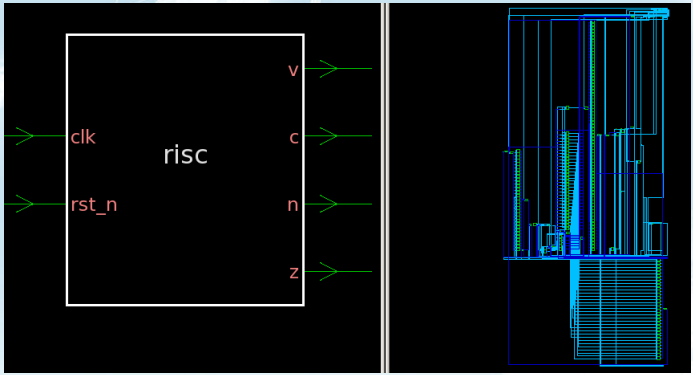
- There is a tool chain from spec. to alerttesting
- Here only introduce *Design Compiler*, used to synthesize RTL code to gate–level.
- *Virtusos→Avant!→Synopsys*

Reading Design

- 夯不啷噹地讀進所有.v 檔



Schematic & Symbol – Top Module



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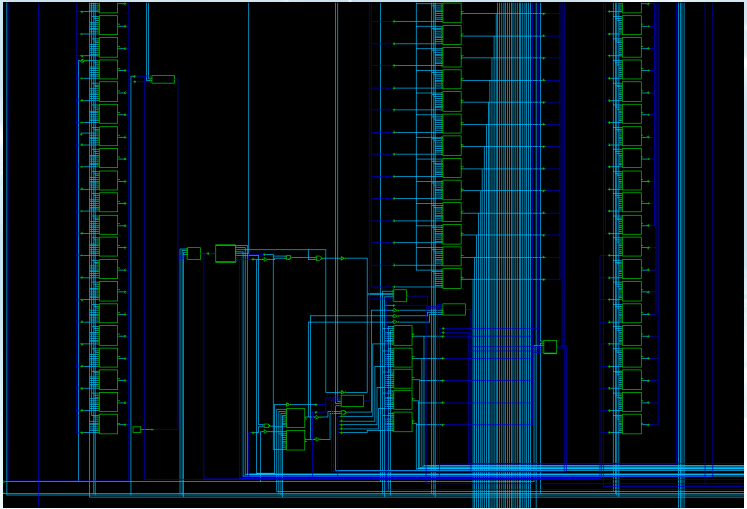

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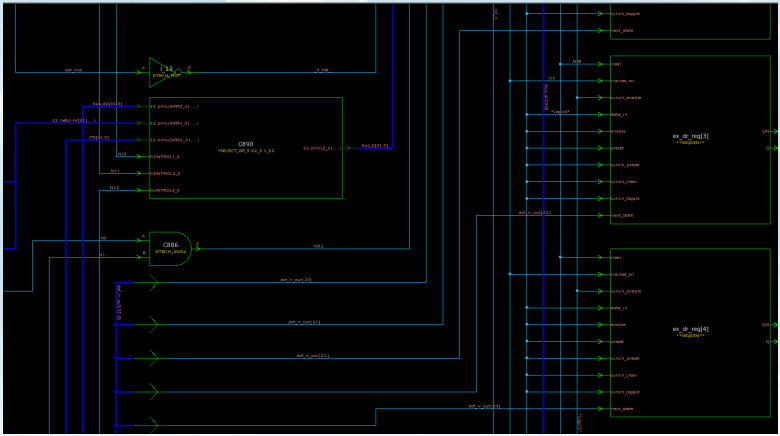
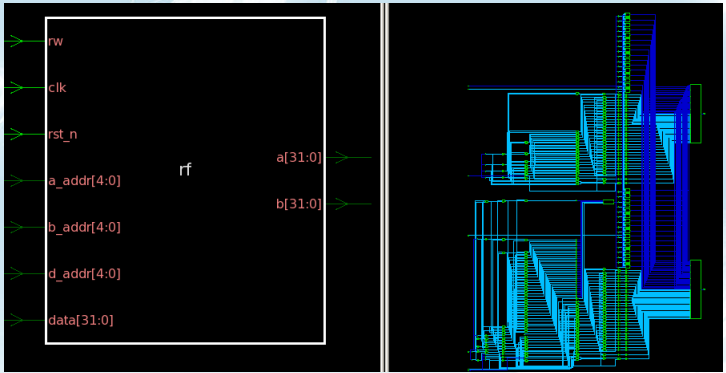
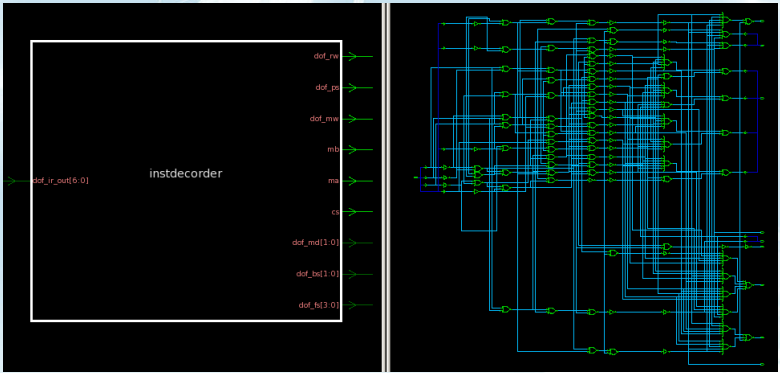


Schematic & Symbol – Register File



Schematic & Symbol – Instruction Decoder



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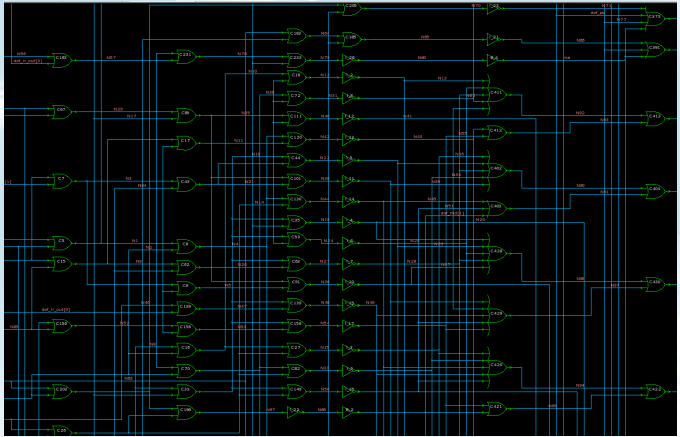
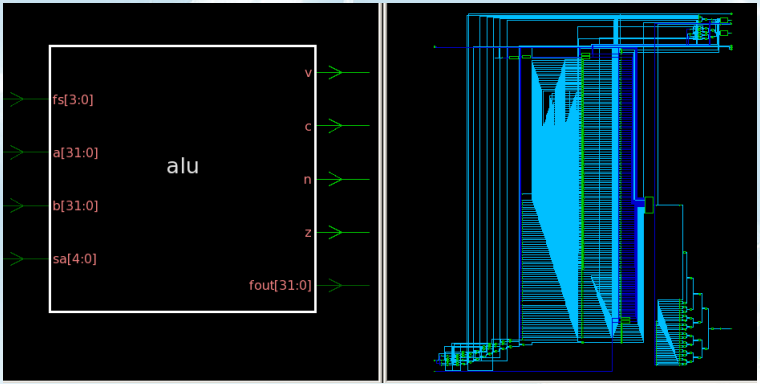
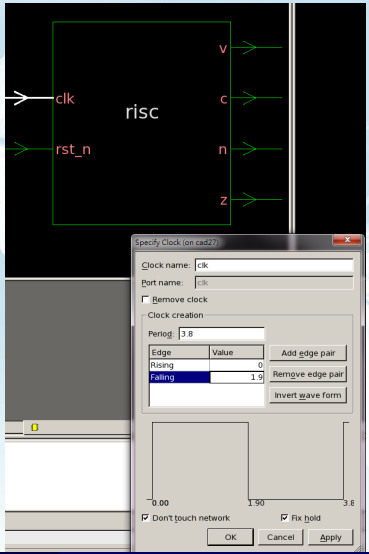


Schematic & Symbol – ALU



Compiling Design – Clock & Wire Load Model



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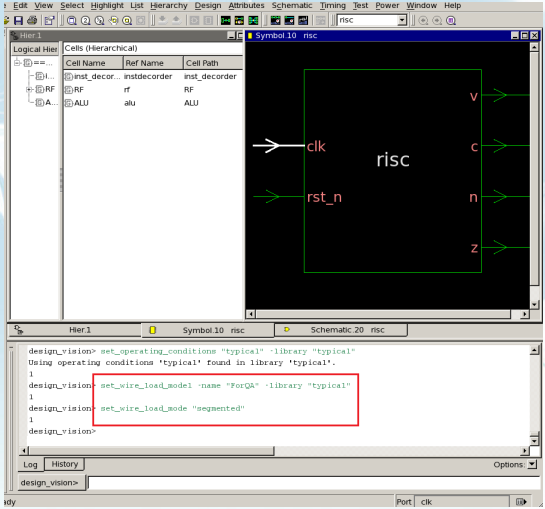
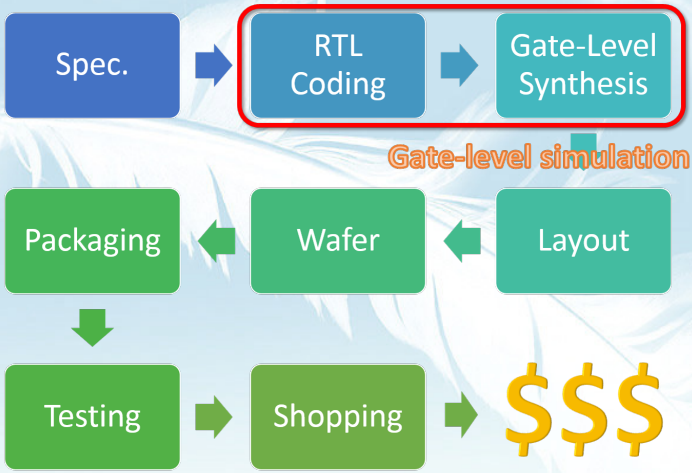


Gate–Level Simulation



Outline

Awful Programming Experience on the self–designing CPU...

- 世界上有 10 種人，懂二進位和不懂二進位的:

tt_bin.dat

```
@0 //This is a program calculating 1+2+3+.......n
0100010_10000_00000__000010000000000  //   main:  ADI  R16, R0, #1024
0010000_00010_10000__000000000000000  //          LD   R2, M[R16]
0000010_00001_00001_00010_0000000000  //   add:   ADD  R1, R1, R2
0100101_00010_00010__0000000000000001 //          SBI  R2, R2, #1
1001000_00000_00010__111111111111100  //          BNZ  R2, add (-4)
0100010_10010_00000__000010000000010  //   done:  ADI  R18, R0, #1026
0100000_00000_10010_00001_0000000000  //          ST   M[R18], R1
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- ARM CPU 架構是 RISC。
- 據說 intel 的 CPU 核心架構也改成 RISC 了，只是外層包上了 RISC–CISC 介面。

Demo

- 如果時間允許且沒出意外的話可以 Demo...

Demo

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- 潛規則：*ncverilog* 是標準中的標準。

Outline

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Linux 架構示意圖

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Linux 架構示意圖

- High–Level programming is ALL based on Low–Level implementation.